depositing a layer of dielectric material; depositing a material comprised of a metal; planarizing and recessing the material comprised of a metal to form a metal gate core in the second gate structure that is adjacent to the layer of dielectric material on at least two surfaces of the metal gate core; and forming a cap layer overlying the layer of dielectric material and the metal gate core. A method as in any above, where a top surface of the metal gate core is not covered by the layer of dielectric material. A method as in any above, where the at least two surfaces comprise at least one sidewall surface and a bottom surface. A method as in any above, where the at least two surfaces does not comprise a top surface of the metal gate core. A method as in any above, further comprising one or more additional aspects of the exemplary embodiments of the invention as described herein.

[0074] (4B) In a further exemplary embodiment, a semiconductor device comprising: a substrate; a gate structure on the substrate, the gate structure comprising a metal gate core that is adjacent to a layer of dielectric material on at least two surfaces of the metal gate core; and a cap layer overlying the layer of dielectric material and the metal gate core.

[0075] The semiconductor device as in any above, where a top surface of the metal gate core is not covered by the layer of dielectric material. The semiconductor device as in any above, where the at least two surfaces comprise at least one sidewall surface and a bottom surface.

[0076] The semiconductor device as in any above, where the at least two surfaces do not comprise a top surface of the metal gate core. The semiconductor device as in any above, further comprising: an interlevel dielectric that at least partially overlies the gate structure; and a borderless contact comprised of a metal. The semiconductor device as in any above, further comprising one or more additional aspects of the exemplary embodiments of the invention as described herein.

[0077] (5) In another exemplary embodiment, and as shown in FIG. **36**, a method (e.g., to fabricate a semiconductor device having a borderless contact) comprising: forming a gate structure on a substrate, the gate structure comprising a layer of dielectric material overlying the substrate, a layer comprised of polycrystalline silicon overlying the layer dielectric material and a first cap layer overlying the layer comprised of polycrystalline silicon (**901**); depositing an interlevel dielectric over the gate structure (**902**); planarizing the interlevel dielectric to expose a top surface of the gate structure (**903**); removing the first cap layer of the gate structure (**904**); forming a fully silicided gate in place of the gate structure (**905**); forming a second cap layer overlying the fully silicided gate (**906**); forming a contact area for the borderless contact by removing a portion of the interlevel dielectric (**907**); and forming the borderless contact by filling the contact area with a material comprised of a metal (**908**).

[0078] A method as in any above, further comprising one or more additional aspects of the exemplary embodiments of the invention as described herein.

[0079] The blocks shown in FIGS. **32-36** further may be considered to correspond to one or more functions and/or operations that are performed in conjunction with one or more components, circuits, chips, apparatus, processors, computer programs and/or function blocks. Any and/or all of the above may be implemented in any practicable solution or arrangement that enables operation in accordance with the exemplary embodiments of the invention as described herein.

[0080] In addition, the arrangement of the blocks depicted in FIGS. **32-36** should be considered merely exemplary and non-limiting. It should be appreciated that the blocks shown in FIGS. **32-36** may correspond to one or more functions and/or operations that may be performed in any order (e.g., any suitable, practicable and/or feasible order) and/or concurrently (e.g., as suitable, practicable and/or feasible) so as to implement one or more of the exemplary embodiments of the invention. In addition, one or more additional functions, operations and/or steps may be utilized in conjunction with those shown in FIGS. **32-36** so as to implement one or more further exemplary embodiments of the invention.

[0081] That is, the exemplary embodiments of the invention shown in FIGS. **32-36** may be utilized, implemented or practiced in conjunction with one or more further aspects in any combination (e.g., any combination that is suitable, practicable and/or feasible) and are not limited only to the steps, blocks, operations and/or functions shown in FIGS. **32-36**.

[0082] The flowchart and block diagrams in FIGS. **32-36** illustrate the architecture, functionality, and operation of possible exemplary implementations of systems, methods and products according to various exemplary embodiments of the invention. In this regard, each block in the flowchart or block diagrams may represent a module, segment or portion of code, which comprises one or more executable instructions for implementing the specified (logical) function(s). It should also be noted that, in some alternative exemplary implementations, the functions noted in the block may occur out of the order noted in the figures. For example, two blocks shown in succession may, in fact, be executed substantially concurrently, or the blocks may sometimes be executed in the reverse order, depending upon the functionality involved. It will also be noted that each block of the block diagrams and/or flowchart illustration, and combinations of blocks in the block diagrams and/or flowchart illustration, can be implemented by special purpose hardware-based systems that perform the specified functions or acts, or combinations of special purpose hardware and computer instructions.

[0083] The exemplary methods and techniques described herein may be used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (i.e., as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (e.g., a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (e.g., a ceramic carrier that has either or both surface interconnections or buried interconnections). The chip is then integrated with other chips, discrete circuit elements and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having numerous components, such as a display, a keyboard or other input device and/or a central processor, as non-limiting examples.

[0084] The terminology used herein is for the purpose of describing particular exemplary embodiments only and is not intended to be limiting of the exemplary embodiments of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated